stored in said first memory unit, wherein said load module includes instructions and data;

a copying unit which copies an instruction code from said load module stored in said first memory unit to a second memory unit out of said plurality of memory units; and

a second address conversion unit which assigns a physical address of said second memory unit to a logical address of the instruction code copied to said second memory unit, wherein

said first address conversion unit comprises a first comparator that compares a requested logical address with said logical address assigned with said physical address of said first memory unit, and

said second address conversion unit comprises a second comparator that compares said requested logical address with said logical address assigned with said physical address of said second memory unit.

4. (Twice Amended) A microprocessor to which a plurality of memory units having physical addresses different from each other are externally connected, said microprocessor comprising:

a first address conversion unit which assigns a physical address of a first memory unit out of said plurality of memory units to a logical address of a load module stored in said first memory unit, wherein said load module includes instructions and data;

a processing unit which temporarily stores and copies an instruction code from said load module stored in said first memory unit to a second memory unit out of said plurality of memory units; and

a second address conversion unit which assigns a physical address of said second memory unit to a logical address of the instruction code stored in said second memory unit, wherein

said first address conversion unit comprises a first comparator that compares a requested logical address with said logical address assigned with said physical address of said first memory unit, and

said second address conversion unit comprises a second comparator that compares said requested logical address with said logical address assigned with said physical address of said second memory unit.

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17. (Twice Amended) A memory device comprising:

a plurality of memory units having physical addresses different from each other;

a first address conversion unit which assigns a physical address of a first memory unit out of said plurality of memories to a logical address of a load module stored in said first memory unit, wherein said load module includes instructions and data;

a copying unit which copies an instruction code from said load module stored in said first memory unit to a second memory unit out of said plurality of memory units; and

a second addr ss conversion unit which assigns a physical address of said second memory unit to a logical address of the instruction code copied to said second memory unit, wherein

said first address conversion unit comprises a first comparator that compares a requested logical address with said logical address assigned with said physical address of said first memory unit, and

said second address conversion unit comprises a second comparator that compares said requested logical address with said logical address assigned with said physical address of said second memory unit.

19 12. (Twice Amended) A memory device comprising:

a plurality of memory units having physical addresses different from each other;

a first address conversion unit which assigns a physical address of a first memory unit out of said plurality of memory units to a logical address of a load module stored in said first memory unit, wherein said load module includes instructions and data;

a processing unit means which temporarily stores and copies an instruction code from said load module stored in said first memory unit to a second memory unit out of said plurality of memory units; and

a second address conversion unit which assigns a physical address of said second memory unit to a logical address of the instruction code stored in said second memory unit, wherein

said first address conversion unit comprises a first comparator that compares a requested logical address with said logical address assigned with said physical address of said first memory unit, and

said second address conversion unit comprises a second comparator that compares said requested logical address with said logical address assigned with said physical address of said second memory unit.

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A marked-up version of the amended claims is enclosed as required by 37 C.F.R. § 1.121.